Translation

PATENT COOPERATION TREATY

PCT/JP2003/011732

PCT

INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY
(Chapter II of the Patent Cooperation Treaty)

(PCT Article 36 and Rule 70)

Applicant's or agent's file reference 142976-013	FOR FURTHER ACTION See Form PCT/IPEA/416	
International application No. PCT/JP2003/011732	International filing date (*day/month/year*) 12 September 2003 (12.09.2003)	Priority date (*day/month/year*) 13 September 2002 (13.09.2002)
International Patent Classification (IPC) or national classification and IPC H02P 5/00		
Applicant TOKYO ELECTRON LIMITED		

1. This report is the international preliminary examination report, established by this International Preliminary Examining Authority under Article 35 and transmitted to the applicant according to Article 36.

2. This REPORT consists of a total of 3 sheets, including this cover sheet.

3. This report is also accompanied by ANNEXES, comprising:

   a. ☐ *(sent to the applicant and to the International Bureau)* a total of _____ sheets, as follows:

      ☐ sheets of the description, claims and/or drawings which have been amended and are the basis of this report and/or sheets containing rectifications authorized by this Authority (see Rule 70.16 and Section 607 of the Administrative Instructions).

      ☐ sheets which supersede earlier sheets, but which this Authority considers contain an amendment that goes beyond the disclosure in the international application as filed, as indicated in item 4 of Box No. I and the Supplemental Box.

   b. ☐ *(sent to the International Bureau only)* a total of (indicate type and number of electronic carrier(s)) _____, containing a sequence listing and/or tables related thereto, in computer readable form only, as indicated in the Supplemental Box Relating to Sequence Listing (see Section 802 of the Administrative Instructions).

4. This report contains indications relating to the following items:

   ☒ Box No. I Basis of the report
   ☐ Box No. II Priority
   ☐ Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
   ☐ Box No. IV Lack of unity of invention
   ☒ Box No. V Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
   ☐ Box No. VI Certain documents cited
   ☐ Box No. VII Certain defects in the international application
   ☐ Box No. VIII Certain observations on the international application

Date of submission of the demand	Date of completion of this report
25 February 2004 (25.02.2004)	03 August 2004 (03.08.2004)
Name and mailing address of the IPEA/JP Facsimile No.	Authorized officer Telephone No.

INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY

International application No.
PCT/JP2003/011732

Box No. I Basis of the report

1. With regard to the **language**, this report is based on the international application in the language in which it was filed, unless otherwise indicated under this item.

☐ This report is based on translations from the original language into the following language _____, which is language of a translation furnished for the purpose of:

☐ international search (under Rules 12.3 and 23.1(b))

☐ publication of the international application (under Rule 12.4)

☐ international preliminary examination (under Rules 55.2 and/or 55.3)

2. With regard to the **elements** of the international application, this report is based on *(replacement sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed" and are not annexed to this report)*:

☒ The international application as originally filed/furnished

☐ the description:

pages _____, as originally filed/furnished

pages* _____ received by this Authority on _____

pages* _____ received by this Authority on _____

☐ the claims:

pages _____, as originally filed/furnished

pages* _____, as amended (together with any statement) under Article 19

pages* _____ received by this Authority on _____

pages* _____ received by this Authority on _____

☐ the drawings:

pages _____, as originally filed/furnished

pages* _____ received by this Authority on _____

pages* _____ received by this Authority on _____

☐ a sequence listing and/or any related table(s) – see Supplemental Box Relating to Sequence Listing.

3. ☐ The amendments have resulted in the cancellation of:

☐ the description, pages _____

☐ the claims, Nos. _____

☐ the drawings, sheets/figs _____

☐ the sequence listing *(specify)*: _____

☐ any table(s) related to sequence listing *(specify)*: _____

4. ☐ This report has been established as if (some of) the amendments annexed to this report and listed below had not been made, since they have been considered to go beyond the disclosure as filed, as indicated in the Supplemental Box (Rule 70.2(c)).

☐ the description, pages _____

☐ the claims, Nos. _____

☐ the drawings, sheets/figs _____

☐ the sequence listing *(specify)*: _____

☐ any table(s) related to sequence listing *(specify)*: _____

* *If item 4 applies, some or all of those sheets may be marked "superseded."*

INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY

International application No.
PCT/JP03/11732

Box No. V **Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement**

1. Statement

Novelty (N)	Claims	1-12	YES
	Claims		NO
Inventive step (IS)	Claims		YES
	Claims	1-12	NO
Industrial applicability (IA)	Claims	1-12	YES
	Claims		NO

2. Citations and explanations (Rule 70.7)

The following documents 1 and 2 were cited in the ISR.

Document 1: JP, 2723764, B2
Document 2: JP, 11-308894, A

Document 1 discloses a semiconductor manufacturing device having controlling means for assisting continuation of wafer processing when supply voltage recovers by storing in processing state storing means a wafer processing state when supply voltage drops, and, when supply voltage recovers, determining the feasibility of automatically continuing the process from the state of abnormal suspension of the wafer processing, and displaying on the operational terminal that the process can be automatically continued when feasible and that the processing chamber must execute processing individually when not feasible.

Document 2 discloses an electric motor processing method at time of power interruption wherein a minimum voltage value of the DC voltage at which normal operations are possible, a minimum permissible voltage of the DC voltage when a minimum voltage that can be permitted is input as a power source, and a power interruption detecting level voltage that is lower than the minimum permissible voltage and higher than the minimum voltage value are individually set, and when the detected value of the DC voltage from the DC voltage detecting means falls lower than the power interruption detecting level voltage while the electric motor is in operation, the motor decelerates until the minimum permissive voltage is exceeded at the decelerating rate set for the electric motor and when the minimum permissible voltage is exceeded return is made to normal control.

The inventions of claims 1-12 of the present application provide a semiconductor manufacturing device as described in document 1, wherein rotation of a motor can be controlled in response to voltage drop at time of instantaneous power interruption.

However, because document 2 discloses controlling a motor in response to voltage drop at time of instantaneous power interruption, the inventions of claims 1-12 of the present application are merely a combining of the inventions disclosed in documents 1 and 2 and could be easily conceived of by a party skilled in the art.

Therefore, the inventions of claims 1-12 do not appear to involve an inventive step.